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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): Betker 8-8-16

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents P O Box 1450 Alexandria VA 22313-1450" [37 CFR 1.8(a)]

on May 11, 2006

Signature: Tina Maurice

Typed or printed name: Tina Maurice

Application Number	Filed
10/081,308	February 20, 2002

First Named Inventor: Betker et al.

Art Unit	Examiner
2195	Kenneth Tang

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- ☐ applicant/inventor
- ☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed (Form PTO/SB/96)
- ☒ attorney or agent of record. Registration number 36,597
- ☐ attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____

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May 11, 2006
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): Betker et al.
Case: 8-8-16
Serial No.: 10/081,308
Filing Date: February 20, 2002
Group: 2195
Examiner: Kenneth Tang

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Commissioner for Patents, P.O. 1450, Alexandria, VA 22313-1450.

Signature: _____ Date: May 11, 2006

Title: Method and Apparatus for Establishing a Bound on the Effect of Task Inteference in a Cache Memory

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MEMORANDUM IN SUPPORT OF
PRE-APPEAL BRIEF REQUEST FOR REVIEW

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The present invention and prior art have been summarized in Applicants' prior responses.

STATEMENT OF GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-2, 5, 7-8, 11, 13-14, 16, and 19 are rejected under 35 U.S.C. §102(e) as being anticipated by Kikuchi (United States Patent Number 6,606,715), claims 3, 9, and 17 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kikuchi in view of Hwu et al. (United States Patent Number 6,681,387), and claims 4, 6, 10, 12, 15, 18, and 20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kikuchi in view of Borg et al. (United States Patent Number 5,274,811).

ARGUMENT

Independent Claims 1, 7, 13 and 16

Independent claims 1, 7, 13, and 16 were rejected under 35 U.S.C. §102(e) as being anticipated by Kikuchi. Regarding claim 1, the Examiner asserts that Kikuchi discloses determining a number (block count / boundary of data blocks) of live frames (blocks during execution) of said application that are coexistent during execution of said application (col. 11, lines 30-67); and establishing said bound based on said number of live frames (block count / boundary of data blocks) (col. 11, lines 30-67). In the Response to Arguments section of the final Office Action, the Examiner asserts that the recitation "establishing a bound on the execution time of an application due to task interference in a shared instruction cache" has not been given patentable weight because the recitation occurs in the preamble. The Examiner further asserts that the broadest reasonable interpretation of a live cache frame is "merely a data block in cache" and that the specification does not contradict this broadest reasonable interpretation of the claim.

Applicants note that Kikuchi is directed to "a device control apparatus and a control method for forming protection data such as a CRC or the like and adding it when user data from an upper apparatus such as a host or the like is buffered into a cache memory." (Col. 1, lines 12-16). Applicants also note that Kikuchi teaches a case

> where the transfer is interrupted in association with the path switching of the fabric 12. In this state, the transfer of the data block and the formation of the protection data cannot be simultaneously performed. On the other hand, in the RAID controllers 18-1 to 18-3 of the invention, a fact that the *transfer of the data block was interrupted is detected during the transfer of the user data from the host and a state of the forming circuit of the protection data at that time is stored. After that, when the restart of the transfer of the data block is detected, the state is returned to the stored circuit state upon interruption and the formation of the protection data is restarted.*"
> (Col. 6, lines 47-59; emphasis added.)

Kikuchi, however, does ***not*** address the issue of *establishing a bound on the execution time of an application due to task interference in a shared instruction cache*, as required by the claims of the present invention. Regarding the Examiner's assertion that the

recitation "establishing a bound on the execution time of an application due to task interference in a shared instruction cache" has not been given patentable weight because the recitation occurs in the preamble, Applicants note that Applicants' argument does not strictly rely on this feature to overcome the cited prior art. Applicants also note, however, that the body of the cited claims require "establishing said bound," and that the preamble recites that the bound is "on the execution time of an application due to task interference in a shared instruction cache." Thus, since the preamble provides completeness for the body of the claims, the preamble should be given patentable weight.

Applicants also note that the present disclosure defines "live cache frames" as, for example, "a cache frame that contains a *block that is accessed in the future without an intervening eviction.* The present invention recognizes that the eviction of blocks from a live frame by an interrupt causes a future miss that would not otherwise occur and that evictions from live frames are the only evictions that cause misses that would not otherwise occur." (Page 2, lines 18-22; emphasis added.)

Clearly, a patentee is entitled to be his own lexicographer. See, e.g., *Rohm & Haas Co. v. Dawson Chemical Co., Inc.*, 557 F. Supp 739, 217 U.S.P.Q. 515, 573 (Tex. 1983); *Loctite Corp. v. Ultraseal Ltd.*, 781 F.2d 861, 228 U.S.P.Q. 90 (Fed. Cir. 1985); and *Fonar Corp. v. Johnson & Johnson*, 821 F.2d 627, 3 U.S.P.Q.2d 1109 (Fed. Cir. 1987).

The interpretation of the term "live cache frame" asserted by the Examiner is inconsistent with the definition provided in the specification and is not how the term would be understood by a person of ordinary skill, based on the specification. When the specification explains and defines a term used in the claims, without ambiguity or incompleteness, there is no need to search further for the meaning of the term. *Multiform Desiccants Inc. v. Medzam Ltd.*, 133 F.3d 1473, 45 U.S.P.Q.2d 1429, 1433 (Fed. Cir. 1998).

Applicants could find no disclosure or suggestion by Kikuchi of ***live frames***, of determining *a number of live frames* of said application that are *coexistent during execution* of said application; and of *establishing a bound based on the number of live frames*. Independent claims 1, 7, 13, and 16 require determining a number of live frames of said application that are

coexistent during execution of said application; and establishing said bound based on said number of live frames.

Thus, Kikuchi does not disclose or suggest determining a number of live frames of said application that are coexistent during execution of said application; and establishing said bound based on said number of live frames, as required by independent claims 1, 7, 13, and 16.

Additional Cited References

Borg et al. was also cited by the Examiner for its disclosure of a cache simulation routine to analyze memory access patterns of a cache. Applicants note that Borg is directed to utilizing "link time code modification to instrument the code which is to be executed, typically comprising plurality of kernel operations and user programs." (See, Abstract.)

Hwu et al. was also cited by the Examiner for its disclosure of detecting and monitoring usage patterns of the data elements in a cache line after access (col. 3, lines 27-54). Applicants note that Hwu is directed to detecting and monitoring program hot spots during execution that may be implemented in hardware. (See, Abstract.)

Applicants could find no disclosure or suggestion by either Borg et al. or Hwu et al. of ***live frames***, of determining *a number of live frames* of said application that are *coexistent during execution* of said application; and of *establishing a bound based on the number of live frames.*

Thus, Borg et al. and Hwu et al., alone or in combination, do not disclose or suggest determining a number of live frames of said application that are coexistent during execution of said application; and establishing said bound based on said number of live frames, as required by independent claims 1, 7, 13, and 16.

Claims 5, 11, 14 and 19

Claims 5, 11, 14, and 19 are rejected under 35 U.S.C. §102(e) as being anticipated by Kikuchi. In the text cited by the Examiner, Kikuchi teaches "a transferred count 122 showing the number of *remaining bytes at the time of transfer interruption*; an executed block count 124 showing the number of *remaining blocks at the time of transfer interruption*; and further, a second OP code 118 including those set values upon transfer interruption as one group." (Col. 9,

lines 51-67; emphasis added.)

Thus, Kikuchi, Hwu et al., and Borg et al., alone or in any combination, do not disclose or suggest wherein said step of establishing said bound further comprises the step of comparing sets that contain live frames of said application with sets accessed by an interrupting task to determine a maximum number of live-frames that may be affected by an interrupting task, as required by claims 5, 11, 14, and 19.

Claims 6, 12, 15 and 20

Claims 6, 12, 15, and 20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kikuchi in view of Borg et al. Applicants, however, could find no disclosure or suggestion by either Kikuchi or Borg to combine the inventions of Kikuchi and Borg.

Thus, Kikuchi, Hwu et al., and Borg et al., alone or in any combination, do not disclose or suggest wherein said step of establishing said bound further comprises the steps of determining an effect of an interrupt at each possible interrupt point and establishing said bound based on a maximum of said effect of an interrupt at each possible interrupt point, as required by claims 6, 12, 15, and 20.

Conclusion

The rejections of the cited claims under sections 102 and 103 in view of Kikuchi, Hwu et al., and Borg et al., alone or in any combination, are therefore believed to be improper and should be withdrawn. The remaining rejected dependent claims are believed allowable for at least the reasons identified above with respect to the independent claims.

The attention of the Examiner to this matter is appreciated.

Respectfully,

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Date: May 11, 2006

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